REMARKS

Claims 1 through 28 are pending in this application.

I. Information Disclosure Statement

The Examiner stated that information disclosure statement (IDS) submitted on 18 April 2001 has been fully considered by the Examiner. However, the Examiner has considered KR1999-48136 and JP9-305381 only to the extent of that which would have been conducted in an ordinary search of the prior art in a proper field of search, specifically, those portions readable and recognizable to the Examiner, as well as statements of relevance disclosed by the applicant on pages 1 and 2 of the information disclosure statement filed 18 April 2001, have been considered, an updated and initialed copy of the information disclosure statement is being provided with this action.

As mentioned in the interview summary record filed on 27 January 2005, such comments are improper as the Examiner is required to fully consider KR1999-48136 and JP9-305381 in the office action. By improperly not considering the entire KR1999-48136 and JP9-305381, paper no. 7 stands to be incomplete and should have the finality removed.

As mentioned in MPEP §706.07, " Before final rejection is in order a clear issue should be developed between the examiner and applicant. To bring the prosecution to as speedy conclusion as possible and at the same time to deal justly by both the applicant and the public...present practice does not sanction hasty and ill-considered final rejections. The applicant who is seeking to define his or her invention in claims that will give him or her the patent protection to which he or she is justly entitled should receive the cooperation of the examiner to that end, and not be prematurely cut

off in the prosecution of his or her application....The examiner should never lose sight of the fact that in every case the applicant is entitled to a full and fair hearing, and that a clear issue between applicant and examiner should be developed, if possible, before appeal." Therefore, the finality must be removed.

II. Claim Rejections - 35 USC § 103

According to MPEP 706.02(j), the following establishes a *prima facie* case of obviousness under 35 U.S.C. §103:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based on applicant's disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

A. Claims 1, 3-5, 10 and 11 are rejected under 35 U.S.C. 103(a) as being anticipated by U.S. Patent 6,075,862 to Yoshida et al, hereafter referred to as Yoshida, in view of "Software-RAID Howto" by Vepstas. The Applicant respectfully traverses.

1. Regarding claim 1:

a. Yoshida fails to teach or suggest a third program stored in the first data storage unit for reinstalling the first program, the third program reading the product key of the first program stored in the second data storage unit, *when a product key from the third program and the product key stored in the second data storage unit are identical* .

The Examiner notes in the response to the arguments, "the installer calls a decryption key retrieval program which searches for an identical ID stored in the decryption key memory unit (Note col. 6 lines 27-40)." However, looking at col. 6, lines 27-40 for instance, Yoshida only states the description key retrieval program searches through the decryption key memory unit and retrieves the decryption key, but there is no teaching of the product key from the decryption key retrieval program and the product key stored unit being identical. This additional step of having a key on the retrieval program itself and checking it with the key on the data storage unit is never made. Yoshida simply retrieves the key from the storage rather than do an error check of the key. Yoshida is then dependent fully on the contents of the memory and then installs based on only the contents of the

memory, but fails to make any sort of check as the presently claimed invention does.

b. In addition, the combined references do not teach or suggest the third program being on the first storage unit while the product key is on a separate data storage unit. Since the Examiner admits that Yoshida makes no teaching of a separate memory unit, but that Vepstas shows a RAID device, then Vepstas must be looked at. However, where is the teaching that one program in particular the third program would be left on the first storage device while the key code would be stored in a separate storage device. Where is the teaching? Simply mentioning that separate memory units can be attached does not make the particular teaching. Why store the key code remotely? Where is the teaching for that? The Federal Circuit has mentioned that "[t]he test for obviousness is not whether the features of one reference may be bodily incorporated into another reference...Rather, we look to see whether combined teachings render the claimed subject matter obvious." *In re Wood*, 599 F.2d 1032, 202 USPQ 171, 174 (CCPA 1979) (citing *In re Bozek*, 416 F.2d 1385, 1390, 163 USPQ 545, 549-50 (CCPA 1969); *In re Mapelsden*, 329 F.2d 321, 322, 141 USPQ 30, 32 (CCPA 1964).

Respectfully, there is absolutely no such teaching of locating one item on the second separate storage unit while still having the other on the original storage unit. An actual teaching must be shown and not just concluded.

Simply stating that the RAID manual teaches of having a separate storage units is still not making teaching of what portions are to be separated. The actual teaching is not made in the RAID

manual.

c. The Examiner uses an improper motivation to reject the present invention. MPEP 706.02(j) states that the teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based on applicant's disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). *In re Dembiczak*, 175 F.3d 994, 50 USPQ.2d 1614 (Fed. Cir. 1999) also states that the showing must be "clear and particular" without broad generalized conclusory statements. "When a rejection depends on a combination of prior art references, there must be some teaching, suggestion, or motivation to combine the references ." In re Rouffet, 149 F.3d 1350, 1355, 47 USPQ2d 1453,1456 (Fed. Cir. 1998). When determining the patentability of a claimed invention which combines several elements, "'the question is whether there is something in the prior art as a whole to suggest the desirability, and thus the obviousness, of making the combination.'" Rouffet, 149 F.3d at 1356, 47 USPQ2d at 1456.

The examiner states that the motivation to combine is that it would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize separate data storage units in the system disclosed by Yoshida, as this would allow the decryption information to be maintained, even in the event of a failure of the other data storage unit. However, the particular teaching of allow the decryption information to be maintained, even in the event of a failure of the other data storage unit is never actually made in Vepstas, but is rather a conjecture based on the Examiner's use of the present invention. The actual teaching must be in the prior art, otherwise, as here the "how to" manual of Vepstas should not be combined with Yoshida as there is not particular teaching actually

in Vepstas. Moreover, the reasoning given by the Examiner does not explain how one particular item or program is on one device while the other particular item or program is on an another. The Examiner cannot just make use a theory of separate storage devices and simply apply it to suit the Examiner's needs.

2. Regarding claim 5 (and also claim 25):

Yoshida does not disclose a first data storage unit comprising a first unit storing the first program, and a second unit storing the third program as claimed where the second unit is a rewritable magnetic disk storage device or an optical storage device.

The Examiner argues that the first unit and second unit alone does not mean a separate storage device, however claim 5 does define the second unit as an actual separate storage device rather than merely a first unit and second unit on the first storage unit. If the second unit is an optical disk in itself, then it cannot be just merely a memory area of the first storage unit, but rather the first storage unit is further divided into two separate physical devices. Therefore, it is clear that Yoshida makes no such claim as the Examiner admits Yoshida does not teach a separate storage unit. Moreover, the dictionary makes no such teaching of having the third program on an optical device while the first on another unit. The dictionary with the RAID definition gives no direction on what program is to be where. The only way, one can show such teaching is by looking improperly at the present invention as the blueprint in the rejection. In addition, merely disclosing an optical disk alone in Yoshida, as the Examiner argues, does not show the separate units having the different programs.

B. Claims 6, 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,075,862 to Yoshida et al, hereafter referred to as Yoshida, in view of "Software-RAID Howto" by Vepstas, further in view of the Microsoft Press Computer Dictionary, Second Edition. The Applicant respectfully traverses.

1. Regarding claim 6:

a. The Examiner improperly uses a dictionary as a reference to reject the present invention. One of the problems is in terms of having a suggestion or motivation to combine or modify the references.

Respectfully, the U.S. Patent Office uses dictionaries for clarifying terminology but not a reference in itself. Otherwise, one can just use a technical dictionary to reject all patent applications. The reason Examiner's do not do this is that it would be an improper rejection.

The Examiner argues that a dictionary can be used as a reference. However, the Examiner is reminded that MPEP 706.02(j) strongly states that the the teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based on applicant's disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

The Examiner admits that Yoshida or Vepstas makes no such teaching or suggestion. Therefore, one can only look to the dictionary and clearly there is no motivation to combine. The Examiner mentions that it would have been obvious to one of ordinary skill in the art at the time the invention was made to represent the product key as a bar code-readable signal, as this would allow

rapid, error-free input of the information as disclosed on page 37 of the dictionary.

However, the dictionary does not make such a motivation and therefore, there is a failure in providing a proper motivation.

Moreover, "Combining prior art references without evidence of such a suggestion, teaching, or motivation simply takes the inventor's disclosure as a blueprint for piecing together the prior art to defeat patentability. *In re Dembiczak*, 175 F.3d 994, 50 USPQ.2d 1614 (Fed. Cir. 1999). The showing must be "clear and particular" without broad generalized conclusory statements. *Id.* There must be specific statements showing the scope of the suggestion, teaching, or motivation to combine the prior art references. *Id.* at 1000. There must be an explanation to what specific understanding or technical principle would have suggested the combination of references. *Id.* Respectfully, stating that to "It would have been obvious to one of ordinary skill in the art at the time the invention was made to represent the product key as a bar code-readable signal, as this would allow rapid, error-free input of the information as disclosed on page 37 of the dictionary." is not a proper suggestion or motivation under the MPEP 706.02(j) because it is not suggested by Yoshida, Vepstas or the dictionary, but rather the present invention is used as a blueprint for the rejection.

Therefore, respectfully, this is an improper rejection.

2. Regarding claim 8:

The Examiner admits that Yoshida nor Vepstas disclose that the storage medium may include

any suitable media for storing electronic instructions, including RAMs and ROMs and magneto-optical disks and Yoshida does not explicitly disclose the second data storage unit being an extended complementary metal-oxide semiconductor random-access memory.

The Examiner again uses improperly the The Microsoft Press Computer Dictionary, Second Edition as a reference to make such disclosures.

However, as shown above, the use of the dictionary here is improper as for instance it does not provide the motivation or suggestion to modify or combine.

The Examiner states that that the use of CMOS RAM was well known in the art at the time of the invention as disclosed on page 77 of the dictionary for the purpose of storing information while using very low power consumption and it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a CMOS RAM in the system disclosed by Yoshida as modified by Vepstas, for the purpose of storing information while using very low power consumption, as disclosed on page 77 of the dictionary.

However, the motivation used by the Examiner is not a motivation to combine with Vepstas or Yoshida, but rather a random reason used by the Examiner uses to combine. With this method, any sort of feature expressed in a dictionary could then be used to combine. However, as a whole, this does not suggest a combination with Yoshida and Vepstas. This short-cut of using a dictionary at assembling a rejection is improper and does not pass the strict procedures set for a 35USC§103 rejection.

3. Regarding claim 9:

Again, the Examiner is improperly using the dictionary as a reference which fails to provide a proper motivation to combine with Yoshida and Vepstas.

The Examiner stated that Microsoft Press Computer Dictionary, Second Edition discloses that the use of CMOS RAM with an auxiliary power source, providing the ability to preserve stored information when power is removed was well known in the art at the time of the invention as disclosed on page 77 of the dictionary (the CMOS RAM is powered by an external battery source).

However, even the definition of CMOS RAM only species that CMOS RAM is useful in hardware components powered by batteries, which does not mean that there is an auxiliary power source as auxiliary is a supplemental reserve source.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a CMOS RAM in the system disclosed by Yoshida as modified by Vepstas, for the purpose of storing and retaining information while using very low power consumption when power is removed from the system. However, the reference as a whole does not teach this. If one were to read the entire dictionary, an entire set of different set of elements may be used, but where is the teaching that this item should be combined rather than the other 100,000 definitions in a dictionary. The entire reference must be looked at and therefore, unless the Examiner has the present invention as a blue print, one cannot know to use the CMOS RAM.

Again, this rejection is highly improper as the dictionary is used as a reference for an obvious type rejection.

C. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent

6,075,862 to Yoshida et al, hereafter referred to as Yoshida, in view of "Software-RAID Howto" by Vepstas, further in view of the Microsoft Press Computer Dictionary, Second Edition. The Applicant respectfully traverses.

Regarding claim 7 (and also claim 27):

a. The Examiner is additionally using Venkatesan to reject claim 7, and therefore, the statement in section 12 is incorrect in that it should also include Venkatesan.

b. The Examiner further argues in the response to the rejection, in the rejection of claim 7, a case of obviousness is created in connection with "When the appropriate decryption key does not exist in the decryption key memory unit ..." in col. 11 lines 21-22. However, this statement does not inherently or explicitly show the product key stored in the third program and the product key stored in the second data storage unit. Yoshida only states "appropriate key" not existing which would be a big conjecture that there is comparison between there is a product key stored in the third program and there is also a product key in the storage unit. Moreover, such comparison is not made. The actual teaching must be taught or suggested, but neither is done here. Again, the Examiner is making a conclusion rather than making a proper finding of fact.

c. In addition, the claim states of "direct input of the product key". Even if Vekatesan is combined with Yoshida, there is not a direct input the product key as Yoshida expressly sends the message to a remote site. There is no teaching in Venkatesan to the effect of direct input. Mere input of a code by a user does not then modify the teaching of Yoshida, because then the user of

Venkatesan will only remotely enter the code rather than directly entering the product key. The references as a whole must be looked, rather than just simply picking and choosing certain elements. according to MPEP §2145, "It is improper to combine references where the references teach away from their combination. *In re Grasselli*, 713 F.2d 731, 743, 218 USPQ 769, 779 (Fed. Cir. 1983). This portion of Yoshida cannot be just ignored because according to MPEP §2141.02, "A prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention. *W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984)."

D. Vepstas reference as related to 35 U.S.C. 103(a) rejection above of claims 1 and 3-11.

Vepstas just discloses that a RAID device distributes data and stores it in a plurality of disks. In Vepstas, if any one of the disks fails, the data on the remaining disks can be used to reconstruct the data that was on the failed disk. In the present invention, program data cannot be reconstructed by the product key and must be restored when the program data was lost.

E. Claims 15, 17 and 19-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,075,862 to Yoshida et al, hereafter referred to as Yoshida in view of U.S. Patent 6,163,841 to Venkatesan et al, hereafter referred to as Venkatesan. The Applicant respectfully traverses.

1. Regarding claim 15:

a. Yoshida or Venkatesan fail to teach or suggest the storage of programs and product keys in a first and second storage units. Two different storage units are never taught or suggested in Yoshida. Moreover, Venkatasan fails to teach what items are to be stored in a different storage unit. The actual teaching is lacking as shown in the response to claim 1. As mentioned above, The Federal Circuit has mentioned that "[t]he test for obviousness is not whether the features of one reference may be bodily incorporated into another reference...Rather, we look to see whether combined teachings render the claimed subject matter obvious." *In re Wood*, 599 F.2d 1032, 202 USPQ 171, 174 (CCPA 1979) (citing *In re Bozek*, 416 F.2d 1385, 1390, 163 USPQ 545, 549-50 (CCPA 1969); *In re Mapelsden*, 329 F.2d 321, 322, 141 USPQ 30, 32 (CCPA 1964). The actual teaching is lacking as it is not clear from Yoshida or Venkatasan where each limitation is stored.

b. The references also fail to teach or suggest comparing the product key read from the second data storage unit with the product key of the first program. The Examiner argues that "when the appropriate decryption key exists in the decryption key memory unit ..." as stated in col. 11 lines 59-60) teaches such. However, merely stating that an "appropriate key existing" is not teaching or suggesting a comparison process from a particular program to another. This criteria is emphasized in MPEP 706.02(j), as the prior art reference (or references when combined) must teach or suggest all the claim limitations. Here it is clear the actual claim limitation is not suggested but a conjecture is made by the Examiner. Here, "appropriate decryption key" does not make such a suggestion.

2. Regarding claim 20:

a. The Examiner stated that Yoshida discloses storing the product key in a specific region of the first data storage unit and the first program continuing to install on the computer system before the step of writing the product key onto a second data storage unit, the product key being written from the product key stored on the first data storage unit ("third computer readable program code means for causing said computer to decrypt the encrypted software by using the decryption key ... and install a decrypted software content into the memory device; and a forth computer readable program code means for causing said computer to store the decryption key acquired ... into the memory device ..." in col. 3 lines 51-59.

However, there is no actual teaching of storing the product key in a *specific region* of the first data storage unit. Yoshida is only stating that the code is stored in a memory device, but the location is not specified.

b. The Examiner states that the system inherently stores the key in a temporary location after it receives the key, so that it can decrypt the software, then the key is saved into memory. This inherency is more like the Examiner using his own knowledge rather than using the reference to reject the claims. Therefore, the Applicant has the right to ask the Examiner produce an actual reference showing such process.

3. Regarding claim 22:

The Examiner stated that Yoshida discloses the step of comparing having the product key of the first program obtained from a third program accommodating the reinstallation of the first program as claimed ("such that the decryption key stored in the memory device is utilizable in decrypting the encrypted software at a time of re-installing the encrypted software" in col. 4 lines 13-15).

However, this disclosure in Yoshida does not teach a comparison step with the comparison according to exactly as claimed in claim 15. The decryption key is merely used, which does not mean it is being checked for errors as the present invention is doing in the comparison step.

F. Claims 12-14, 16, 18 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,075,862 to Yoshida et al, hereafter referred to as Yoshida in view of U.S. Patent 6,163,841 to Venkatesan et al, hereafter referred to as Venkatesan, further in view of the Microsoft Press Computer Dictionary, Second Edition. The Applicant respectfully traverses.

1. Regarding claim 12:

a. Again, as shown above, the use of the dictionary as a reference is improper in this rejection. The motivation or suggestion to combine is not a proper one and looking at the dictionary as whole, the Applicant is skeptical that such an element would be chosen from the entire dictionary without looking at the present invention for guidance as to what element to read in the thousands of words of the dictionary.

2. Regarding claim 13:

The Examiner stated that rejection of claim 12 is incorporated, and further, note the rejection of claim 7. However, claim 7 does not include the product key storage accommodated in the extended complementary metal-oxide semiconductor random access memory. The product key being accommodated in the CMOS RAM cannot be taught by dictionary. There must be an actual teaching of the product key being stored in such media rather than just defining what a CMOS RAM is. Again, this is a highly improper rejection.

3. Regarding claim 16:

Again, the use of the dictionary to teach the bar code reader inputting the product key is unorthodox and it still does not teach the bar code reader being used for that purpose.

4. Regarding claim 18:

The Examiner profuse use of the dictionary for rejection purposes is quite improper. Simply using a definition of checksum is not a proper rejection. None of the other references as the Examiner admits even mentions the use of a checksum.

5. Regarding claim 28:

Once again, the use of the dictionary to teach the CMOS with a backup power source is

improper as mentioned above. Moreover, there is not actual teaching of how the CMOS will be used in either the dictionary or the other references, and therefore, all the claimed limitations are not taught or suggested. Simply giving a definition of a CMOS is not enough to satisfy the Examiner's burden of providing a *prima facie* case of obviousness. The PTO has the **burden of proof, by a preponderance of the evidence**, to show that an applicant is not entitled to a patent because the claimed subject matter is anticipated by, or is obvious from, the art of record. A patent applicant is entitled to a patent "unless" the PTO establishes otherwise. See, e.g., *In re Dembiczak*, 175 F.3d 994, 1001, 50 U.S.P.Q.2d 1614 (Fed. Cir. 1999); *In re Epstein*, 32 F.3d 1559, 1564 (Fed. Cir. 1994); *In re Rijckeart*, 9 F.3d 1551, 1552, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); *In re Fine*, 837 F.2d 1071, 1074, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988). Here, as shown in claim 28 and all the other claims, it is clear that the Examiner has failed in his burden of proof.

III. Incomplete Office Action under 37 C.F.R. §1.104

With regard to rejected claim 2, the Examiner has failed to provide a specific reason for the rejection. There was no reference cited against claim 2. Therefore, this rejection is incomplete under 37 C.F.R. §1.104. In addition, because of MPEP 706.07, the finality of the rejection should be withdrawn.

IV. Summary of the Telephone Interview

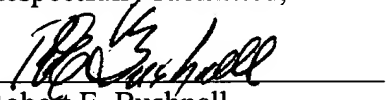
On 22 and 25 April 2005, S. Sahota (Reg. No.47,051) contacted the Examiner and Supervisor concerning the failure to provide a specific reason for rejection of claim 2 and requested a

clarification of paper no. 7, preferably with a supplemental Office action. There was no reference cited against claim 2. The Applicant appreciates the Examiner's and Supervisor's consideration concerning this matter.

In view of the foregoing remarks, all claims are deemed to be allowable and this application is believed to be in condition to be passed to issue. If there are any questions, the examiner is asked to contact the applicant's attorney.

No fee is incurred by this Response. Should there be a deficiency in payment, or should other fees be incurred, the Commissioner is authorized to charge Deposit Account No. 02-4943 of Applicant's undersigned attorney in the amount of such fees.

Respectfully submitted,



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